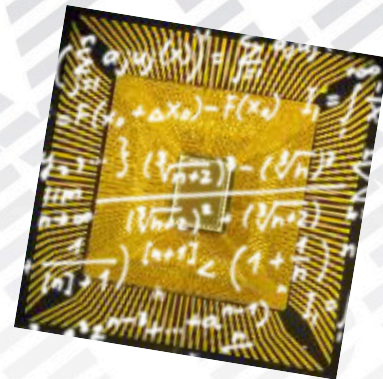


# Decimal and Binary QP Precision Floating Point on IBM z13™



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# Outline

- Motivation
- Pipeline overview of the DQE
- Implementation highlights
- Performance results
- Conclusion



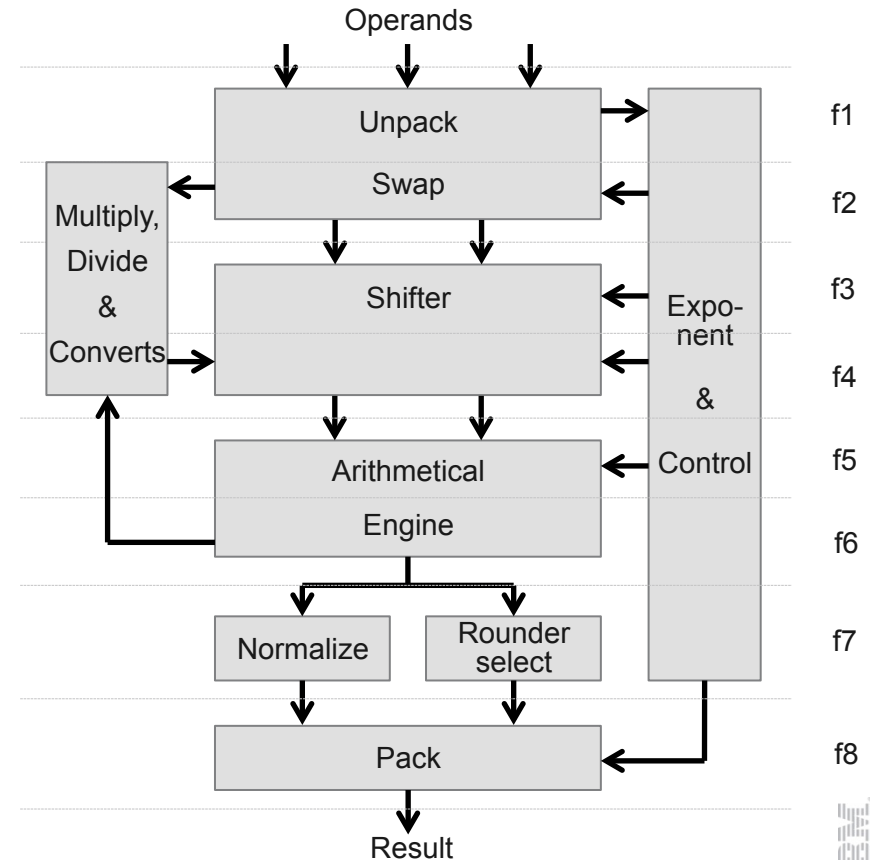
# Workloads Requirement

- Decimal computation
  - Widely used for workload in Banking, Accounting and traditional Insurance code
  - Cobol, PL/1 and JAVA Big Decimal, C/C++
- Binary Quad Precision
  - Big Data Analytics, Risk Assessment code
  - Increased mathematical stability of the algorithms
  - Big ILOG installation: Quad precision in critical routines allows 18% faster convergence
- New hardware design point to support traditional and emerging workload
- Implementation
  - Area and power matters → Highly efficient design required
  - Combine and share logic between decimal and binary FP and BCD functions



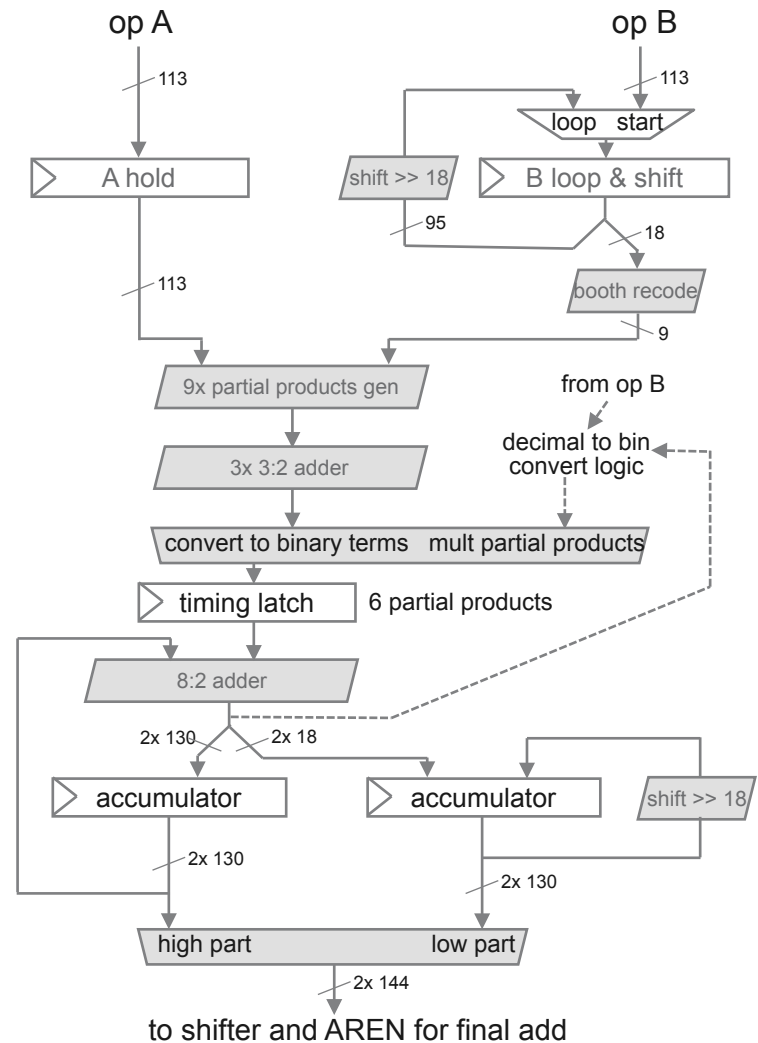
# Decimal and Binary Quad Precision Engine

- 8 cycles pipeline for pipelined ops
- Full HW support for subnormal numbers
- Multi-cycles operations
  - Decimal Multiply and Divide
  - Binary Multiply
  - Converts Decimal $\leftrightarrow$ Binary
- Supports 7 FP formats and BCD format
  - DFP: QP (34d), DP (16d), SP (7d)
  - BFP: QP (113b)
  - HFP: QP (28d), DP (14d), SP (7d)
  - BCD: 31d



# DQE – Binary Multiplier

- Computes 18bits per cycle
- Booth encoding to reduce to 9 partial prods
- Accumulation in redundant format
- Final add, shift and round
  
- Circuit reused for converts from decimal to binary



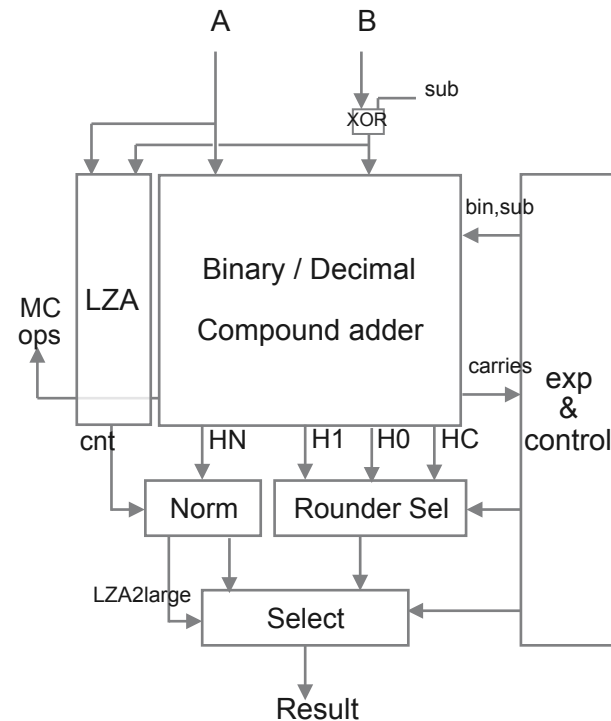
# DQE – Arithmetical Engine

- QP compound adder (144bit wide)
- Supports binary, hex and decimal add/sub
  - Sign magnitude arithmetic via end-around-carry
  - Uses injection rounding

$$RRes = \begin{cases} A+B & \text{if add} \\ A-B & \text{if sub and } (A > B) \\ B-A & \text{if sub and } (A \leq B) \end{cases} = \begin{cases} H0/H1 & \text{if add} \\ H1/H0 & \text{if sub and ( eac or bin)} \\ HC/H1 & \text{if sub and (!eac or !bin)} \end{cases}$$

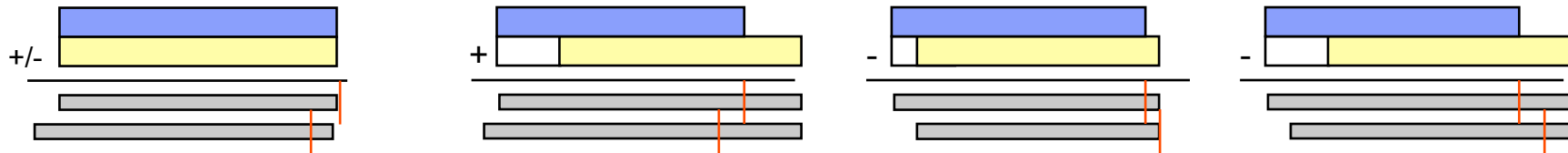
- Normalizer (bin only)

$$NRes = \begin{cases} A+B & \text{if add or special} \\ A-B & \text{if sub and } (A > B) \\ B-A & \text{if sub and } (A \leq B) \end{cases} = \begin{cases} H0 & \text{if add (deno) or special} \\ H1 & \text{if sub and bin and eac} \\ HC & \text{if sub and bin and !eac} \end{cases}$$



# DQE – Rounder or Normalizer

- Normalizer and rounder in parallel to save delay



$eA = eB$	$eA = eB+1$	$eA > eB+1$
Add: $A, B \geq NMIN$ <ul style="list-style-type: none"> <li>• Max 1 extra bit <math>\Rightarrow</math> RND</li> <li>• <math>A+B \geq NMIN</math> <math>\Rightarrow</math> no UNF</li> </ul>	Add: A is normal, B get aligned <ul style="list-style-type: none"> <li>• Max 1 extra bit <math>\Rightarrow</math> RND</li> <li>• <math>A+B \geq NMIN</math> <math>\Rightarrow</math> no UNF</li> </ul>	
Add: $A, B < NMIN$ <ul style="list-style-type: none"> <li>• Result max. 1.fff <math>\Rightarrow</math> exact, no OVF</li> <li>• May UNF <math>\Rightarrow</math> NORM</li> </ul>		
Sub: <ul style="list-style-type: none"> <li>• No align, <math>res \leq A \Rightarrow</math> exact, no OVF</li> <li>• May UNF <math>\Rightarrow</math> NORM</li> </ul>	Sub: Result keeps MSB <ul style="list-style-type: none"> <li>• B get aligned <math>\Rightarrow</math> RND</li> <li>• <math>A-B \geq NMIN</math> <math>\Rightarrow</math> no UNF</li> </ul>	Sub: <ul style="list-style-type: none"> <li>• A is 1.ffff, B is 0.0fff <math>\Rightarrow</math> loose <math>\leq</math> 1 bit</li> <li>• Res max 1 bit shift <math>\Rightarrow</math> RND</li> <li>• <math>eA &gt; eMIN+1</math> <math>\Rightarrow</math> no UNF</li> </ul>
	Sub: Result with cancellation <ul style="list-style-type: none"> <li>• B get aligned by 1 bit</li> <li>• mantissa has max p bits <math>\Rightarrow</math> NORM</li> </ul>	





# DQE – Performance Comparison

- Binary FP QP performance results on the DQE compared to previous generation
  - Latency: # cycles between dependent instructions
  - CPI: # cycles before a new independent instruction can start

	Latency zEC12™	Latency z13™	CPI zEC12™	CPI z13™
Add/Sub	35	11	28	1.5
Multiply	55-97	23	48-90	7.5
Divide*	~165	49	~158	21
Sqrt*	~170	66	~163	24

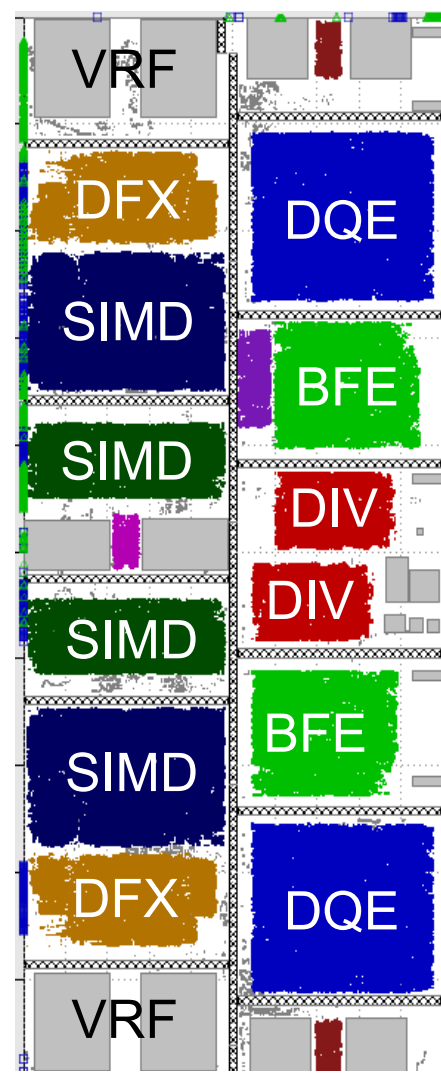
\* Divide/Square Root executed in the Divide Engine, not in the DQE.

- Separated Div/SQRT and DQE engine to allow parallel execution
- About 3x better latency and 7-20x better CPI over zEC12™



# Summary

- Highly efficient Decimal and Binary Quad Precision Design
- Shared logic supporting 8 different data types
- Runs at 5GHz in 22nm SOI Technology
- Widely improved performance over previous generation
- Protected by residue or parity to achieve high reliability
- Total area of the Vector FP Unit: 3.9 mm<sup>2</sup>



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