Decimal and Binary QP Precision Floating Point on IBM z13™

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Outline

• Motivation
• Pipeline overview of the DQE
• Implementation highlights
• Performance results
• Conclusion
Workloads Requirement

• Decimal computation
  • Widely used for workload in Banking, Accounting and traditional Insurance code
  • Cobol, PL/1 and JAVA Big Decimal, C/C++

• Binary Quad Precision
  • Big Data Analytics, Risk Assessment code
  • Increased mathematical stability of the algorithms
  • Big ILOG installation: Quad precision in critical routines allows 18% faster convergence

• New hardware design point to support traditional and emerging workload

• Implementation
  • Area and power matters → Highly efficient design required
  • Combine and share logic between decimal and binary FP and BCD functions
Decimal and Binary Quad Precision Engine

- 8 cycles pipeline for pipelined ops
- Full HW support for subnormal numbers
- Multi-cycles operations
  - Decimal Multiply and Divide
  - Binary Multiply
  - Converts Decimal<->Binary
- Supports 7 FP formats and BCD format
  - DFP: QP (34d), DP (16d), SP (7d)
  - BFP: QP (113b)
  - HFP: QP (28d), DP (14d), SP (7d)
  - BCD: 31d
DQE – Binary Multiplier

- Computes 18 bits per cycle
- Booth encoding to reduce to 9 partial products
- Accumulation in redundant format
- Final add, shift and round
- Circuit reused for converts from decimal to binary
DQE – Arithmetical Engine

- **QP compound adder** (144bit wide)
- **Supports binary, hex and decimal add/sub**
  - Sign magnitude arithmetic via end-around-carry
  - Uses injection rounding

\[
RRes = \begin{cases} 
A+B & \text{if add} \\
A-B & \text{if sub and } (A > B) \\
B-A & \text{if sub and } (A \leq B) 
\end{cases} = \begin{cases} 
H0/H1 & \text{if add} \\
H1/H0 & \text{if sub and (eac or bin)} \\
HC/H1 & \text{if sub and (!eac or !bin)} 
\end{cases}
\]

- **Normalizer** (bin only)

\[
NRes = \begin{cases} 
A+B & \text{if add or special} \\
A-B & \text{if sub and } (A > B) \\
B-A & \text{if sub and } (A \leq B) 
\end{cases} = \begin{cases} 
H0 & \text{if add (deno) or special} \\
H1 & \text{if sub and bin and eac} \\
HC & \text{if sub and bin and !eac} 
\end{cases}
\]
DQE – Rounder or Normalizer

- Normalizer and rounder in parallel to save delay

<table>
<thead>
<tr>
<th>eA = eB</th>
<th>eA = eB+1</th>
<th>eA &gt; eB+1</th>
</tr>
</thead>
</table>
| Add: A, B ≥ NMIN  
  - Max 1 extra bit  => RND  
  - A+B ≥ NMIN  => no UNF | Add: A is normal, B get aligned  
  - Max 1 extra bit  => RND  
  - A+B ≥ NMIN  => no UNF | Add: A-B ≥ NMIN  => no UNF |
| Add: A, B < NMIN  
  - Result max. 1.fff => exact, no OVF  
  - May UNF  => NORM | Sub: Result keeps MSB  
  - B get aligned  => RND  
  - A-B ≥ NMIN  => no UNF | Sub:  
  - A is 1.ffff, B is 0.0fff => loose ≤ 1 bit  
  - Res max 1 bit shift  => RND  
  - eA > eMIN+1  => no UNF |
| Sub:  
  - No align, res ≤ A => exact, no OVF  
  - May UNF  => NORM | Sub: Result with cancelation  
  - B get aligned by 1 bit  
  - mantissa has max p bits  => NORM |
DQE – Sharing of the Adder Logic

- **Dec/bin shared logic**
- **Dec only add/sub logic**
- **Dec only sub logic**
- **Bin only logic**

For each digit:

\[
\begin{align*}
S_{0i} & = \text{dec only add/sub logic} \\
S_{1i} & = \text{dec only sub logic} \\
H_{0i} & = \text{bin only logic}
\end{align*}
\]
DQE – Performance Comparison

• Binary FP QP performance results on the DQE compared to previous generation
  • Latency: # cycles between dependent instructions
  • CPI: # cycles before a new independent instruction can start

<table>
<thead>
<tr>
<th></th>
<th>Latency zEC12™</th>
<th>Latency z13™</th>
<th>CPI zEC12™</th>
<th>CPI z13™</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add/Sub</td>
<td>35</td>
<td>11</td>
<td>28</td>
<td>1.5</td>
</tr>
<tr>
<td>Multiply</td>
<td>55-97</td>
<td>23</td>
<td>48-90</td>
<td>7.5</td>
</tr>
<tr>
<td>Divide*</td>
<td>~165</td>
<td>49</td>
<td>~158</td>
<td>21</td>
</tr>
<tr>
<td>Sqrt*</td>
<td>~170</td>
<td>66</td>
<td>~163</td>
<td>24</td>
</tr>
</tbody>
</table>

* Divide/Square Root executed in the Divide Engine, not in the DQE.

• Separated Div/SQRT and DQE engine to allow parallel execution
• About 3x better latency and 7-20x better CPI over zEC12™
Summary

• Highly efficient Decimal and Binary Quad Precision Design
• Shared logic supporting 8 different data types
• Runs at 5GHz in 22nm SOI Technology
• Widely improved performance over previous generation
• Protected by residue or parity to achieve high reliability

• Total area of the Vector FP Unit: 3.9 mm²
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